ESDALC6V1M3

Dual low capacitance Transil™ array for ESD protection

Features

- 2 unidirectional, low capacitance Transil diodes
- Better than IEC 61000-4-2 standard (ESD protection: 11 kV contact discharge)
- Breakdown Voltage V_{BR} = 6.1 V min
- Low diode capacitance (11 pF typ at 0 V)
- Low leakage current < 0.5 µA
- Very small PCB area: 0.6 mm²
- RoHS compliant

Benefits

- High ESD protection level
- High integration
- Suitable for high density boards

Complies with the following standards

- IEC61000-4-2 level 4:
  - 15 kV (air discharge)
  - 8 kV (contact discharge)
- MIL STD 883G-Method 3015-7: class 3B
  - HBM (human body model)

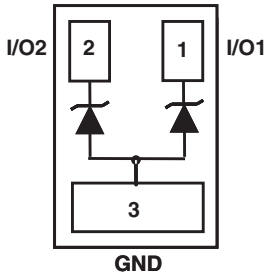
Applications

Where transient overvoltage protection in ESD sensitive equipment is required, such as:

- Computers
- Printers
- Communication systems
- Cellular phone handsets and accessories
- Video equipment

SOT883
(JEDEC MO-236AA compliant)

Figure 1. Functional diagram



Underside view

Description

The ESDALC6V1M3 is a monolithic array designed to protect 1 line or 2 lines against ESD transients.

The device is ideal for applications where both reduced line capacitance and board space saving are required.

TM: Transil is a trademark of STMicroelectronics

1 Characteristics

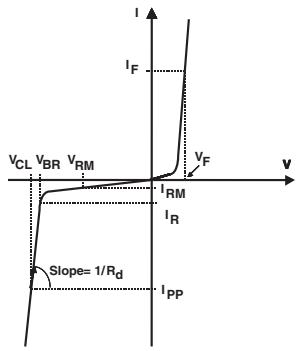
Table 1. Absolute ratings (T_{amb} = 25 °C - limiting values)

Symbol	Parameter			Value	Unit
V_{PP}	ESD discharge	IEC61000-4-2 air discharge IEC61000-4-2 contact discharge		± 15 ± 11	kV
P_{PP}	Peak pulse power dissipation (8/20 µs)(1)		T_j initial = T_{amb}	30	W
I_{pp}	Repetitive peak pulse current (8/20 µs)			3	A
T_j	Junction temperature			125	°C
T_{stg}	Storage temperature range			-55 + 150	°C
T_L	Maximum lead temperature for soldering during 10 s			260	°C
T_{OP}	Operating temperature range			-40 + 125	°C

1. For a surge greater than the maximum values, the diode will fail in short-circuit.

Table 2. Electrical characteristics (T_{amb} = 25 °C)

Symbol	Parameter
V_{RM}	Stand-off voltage
V_{BR}	Breakdown voltage
V_{CL}	Clamping voltage
I_{RM}	Leakage current @ V_{RM}
I_{PP}	Peak pulse current
αT	Voltage temperature coefficient
V_F	Forward voltage drop



Parameter	Test condition	Min	Typ	Max	Unit
V_{BR}	I_R = 1 mA	6.1		7.2	V
I_{RM}	V_{RM} = 5 V			0.5	µA
R_d			1.1		Ω
αT	I_R = 1 mA			4.2	10^{-4}/°C
C	V_R = 0 V, F = 1 MHz, V_{OSC} = 30 mV		11		pF

Figure 2. S21 attenuation measurement results of each channel

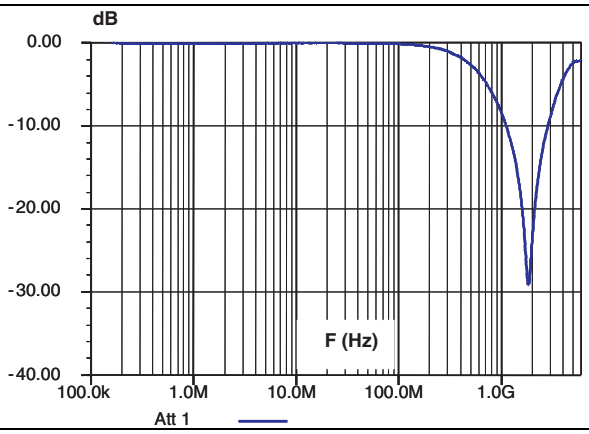


Figure 3. Analog crosstalk measurements between channels

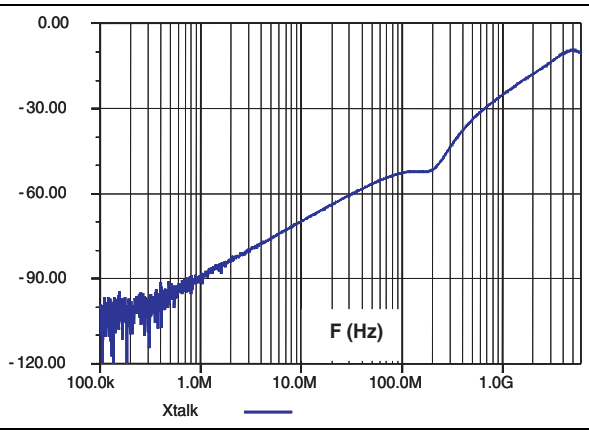


Figure 4. ESD response to IEC61000-4-2 (+15 kV air discharge) on each channel

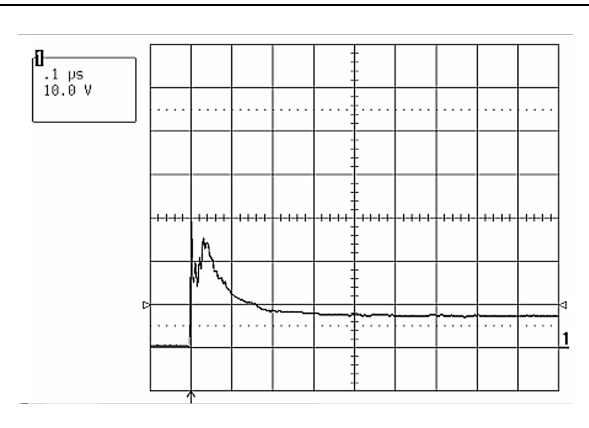


Figure 5. ESD response to IEC61000-4-2 (-15 kV air discharge) on each channel.

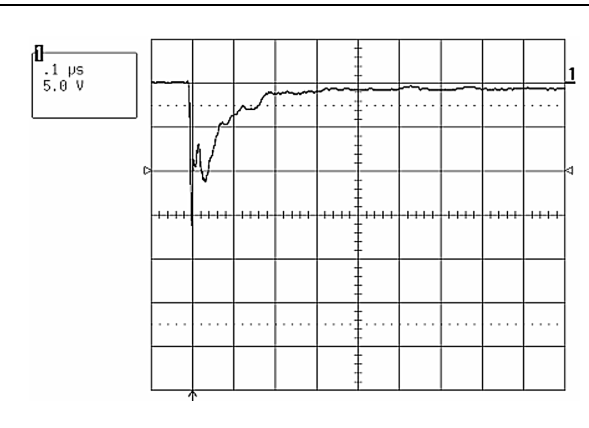


Figure 6. Relative variation of peak pulse power versus initial junction temperature

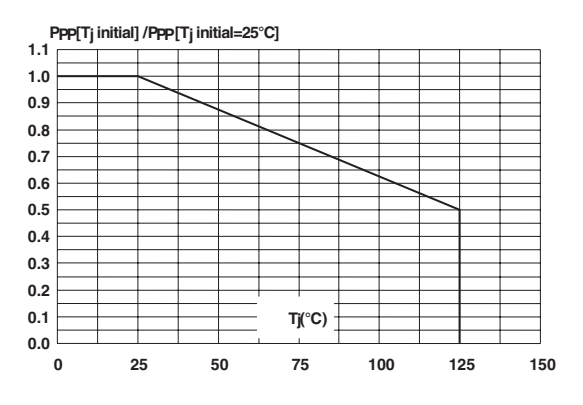


Figure 7. Peak pulse power versus exponential pulse duration

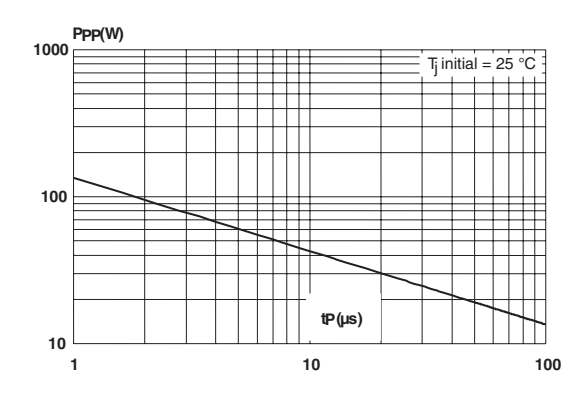


Figure 8. Clamping voltage versus peak pulse current (typical values)

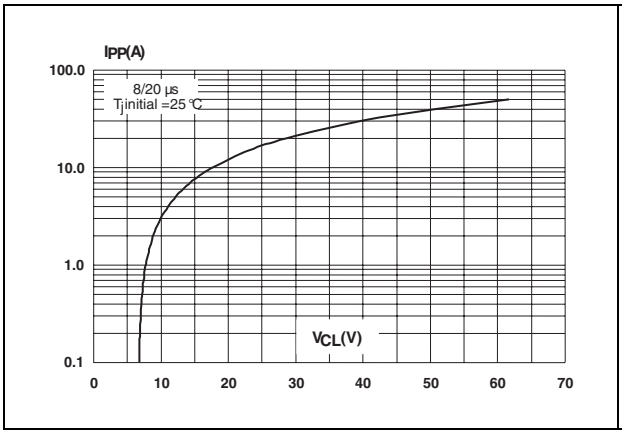


Figure 9. Forward voltage drop versus peak forward current (typical values)

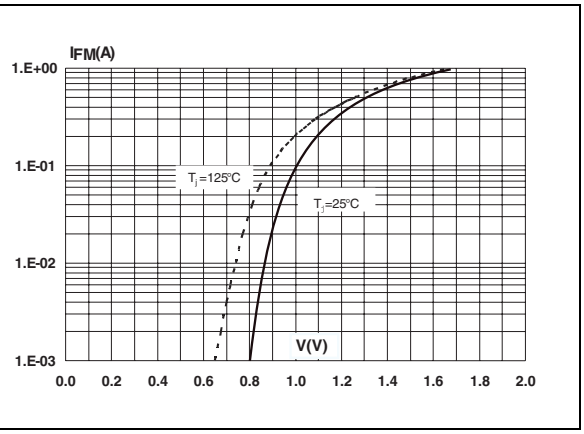


Figure 10. Junction capacitance versus reverse voltage applied (typical values)

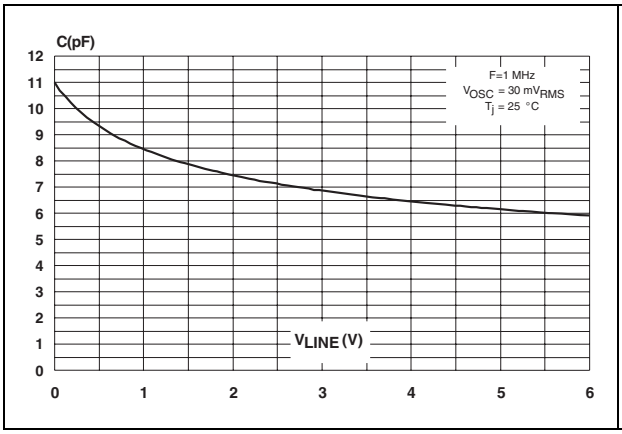
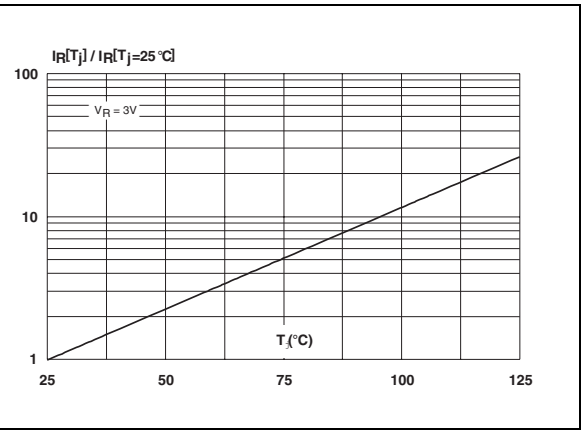
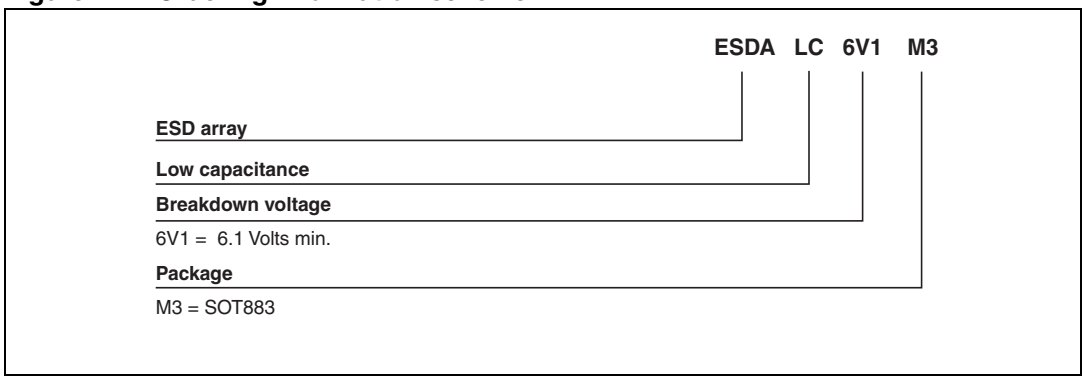


Figure 11. Relative variation of leakage current versus junction temperature (typical values)



2 Ordering information scheme

Figure 12. Ordering information scheme

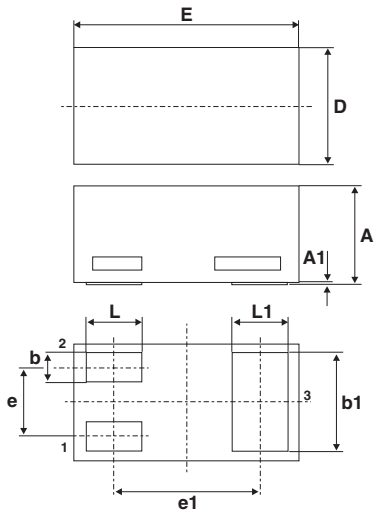


3 Package information

- Epoxy meets UL94, V0

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at *www.st.com*.

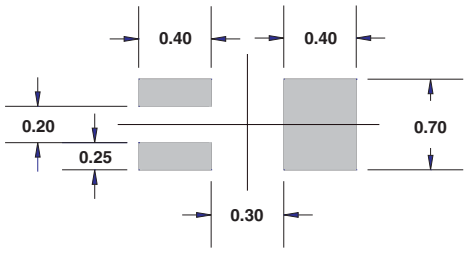
Table 3. SOT883 dimensions



Ref.	Dimensions					
	Millimetres			Inches		
	Min	Typ	Max	Min	Typ	Max
A	0.45		0.52	0.18		0.2
A1	0.00		0.05	0.00		0.02
b	0.10	0.15	0.20	0.04	0.06	0.08
b1	0.45	0.50	0.55	0.18	0.20	0.22
D		0.60			0.24	
E		1.00			0.39	
e		0.35			0.14	
e1		0.65			0.26	
L	0.20	0.25	0.30	0.08	0.10	0.12
L1	0.20	0.25	0.30	0.08	0.10	0.12

Note: Product marking may be rotated by 90° for assembly plant differentiation. In no case should this product marking be used to orient the component for its placement on a PCB. Only pin 1 mark is to be used for this purpose.

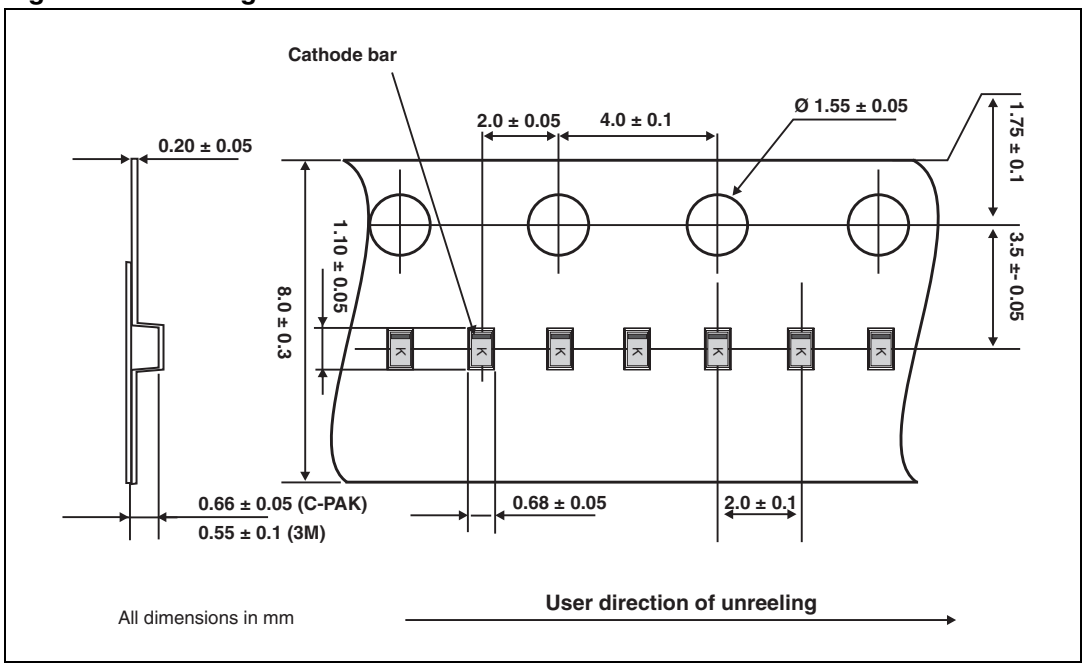
Figure 13. Footprint



All dimensions in mm

Figure 14. Marking

Figure 15. Packing information

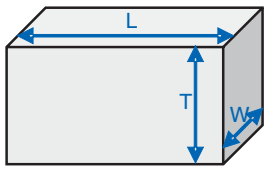


4 Recommendation on PCB assembly

4.1 Stencil opening design

1. General recommendation on stencil opening design
   a) Stencil opening dimensions: L (Length), W (Width), T (Thickness).

Figure 16. Stencil opening dimensions



   b) General design rule

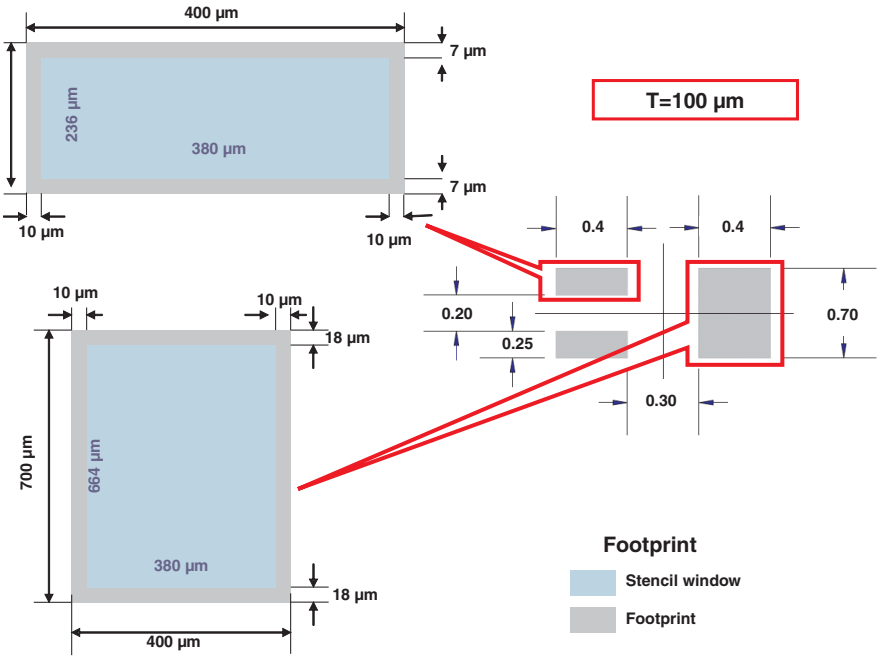
   Stencil thickness (T) = 75 ~ 125 µm

$$\text{Aspect Ratio} = \frac{W}{T} \geq 1.5$$

$$\text{Aspect Area} = \frac{L \times W}{2T(L+W)} \geq 0.66$$

2. Reference design
   a) Stencil opening thickness: 100 µm
   b) Stencil opening for leads: Opening to footprint ratio 90%.

Figure 17. Recommended stencil window position



4.2 Solder paste

1. Halide-free flux qualification ROL0 according to ANSI/J-STD-004.
2. “No clean” solder paste is recommended.
3. Offers a high tack force to resist component movement during high speed.
4. Solder paste with fine particles: powder particle size is 20-45 µm.

4.3 Placement

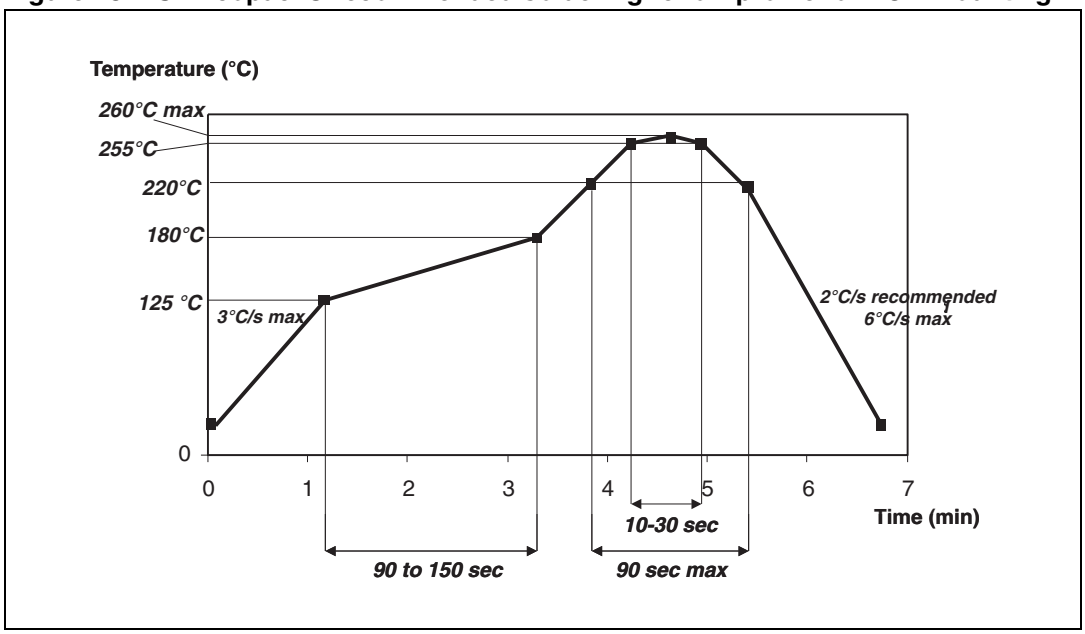
1. Manual positioning is not recommended.
2. It is recommended to use the lead recognition capabilities of the placement system, not the outline centering.
3. Standard tolerance of ± 0.05 mm is recommended.
4. 3.5 N placement force is recommended. Too much placement force can lead to squeezed out solder paste and cause solder joints to short. Too low placement force can lead to insufficient contact between package and solder paste that could cause open solder joints or badly centered packages.
5. To improve the package placement accuracy, a bottom side optical control should be performed with a high resolution tool.
6. For assembly, a perfect supporting of the PCB (all the more on flexible PCB) is recommended during solder paste printing, pick and place and reflow soldering by using optimized tools.

4.4 PCB design preference

1. To control the solder paste amount, the closed via is recommended instead of open vias.
2. The position of tracks and open vias in the solder area should be well balanced. The symmetrical layout is recommended, in case any tilt phenomena caused by asymmetrical solder paste amount due to the solder flow away.

4.5 Reflow profile

Figure 18. ST Ecopack® recommended soldering reflow profile for PCB mounting



Note: Minimize air convection currents in the reflow oven to avoid component movement.

5 Ordering information

Table 4. Ordering information

Order code	Marking	Package	Weight	Base qty	Delivery mode
ESDALC6V1M3	K(1)	SOT883	0.96 mg	3000	Tape and reel

1. The marking can be rotated by 90° to differentiate assembly location

6 Revision history

Table 5. Document revision history

Date	Revision	Changes
04-Aug-2005	1	Initial release.
23-May-2006	2	Reformated to current standards. Added soldering reflow profile diagram.
16-Jun-2006	3	Updated tape and reel illustration (Figure 14).
18-Feb-2007	4	Reformatted to current standards. Added notes on marking rotation. Updated tape and reel illustration - *Figure 15*. Added *Section 4: Recommendation on PCB assembly*. Updated footprint in *Figure 13*.

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